IN THE SPECIFICATION:

Please amend the first full paragraph on page 2 as follows:

This application is a divisional application of United States Patent Application Serial No. 08/677,514, filed on July 10, 1996, now U.S. ~~Pat.~~ Patent 6,107,183, issued August 22, 2000, which is incorporated herein by reference.

Please amend the third full paragraph on page 3 as follows:

One way to gain some of the benefits of low dielectric constant materials is shown in Figure 1. Figure 1 is a partial ~~cross-section~~ cross-section of a partially formed integrated circuit device. A substrate or ~~lower~~ underlying layer 12 has a first dielectric layer 14 comprised of a traditional dielectric material such as silicon dioxide. Lines of conductive material 16, typically metal, overlie first dielectric layer 14. A material 18 with a dielectric constant lower than that of silicon dioxide ~~18 is~~ is located in between lines of conductive material 16. Lines of conductive material 16 together with low dielectric constant ~~dielectric~~ material 18 are covered by a second dielectric layer 21 comprised of a traditional dielectric material such as silicon dioxide. Second dielectric layer 21 together with first dielectric layer 14 isolate low dielectric constant ~~dielectric~~ material 18 from other portions of the integrate circuit. Second dielectric layer 21 allows further processing, including formation of contact holes for contacting lines of conductive material 16 such as contact hole 46, without exposing low dielectric constant material 18 to processing agents.

Please amend the second full paragraph on page 7 as follows:

Figure 1 is a partial ~~cross-section~~ cross-section of a partially formed integrated circuit device.

Please amend the third full paragraph on page 7 as follows:

Figure 2 is a partial ~~cross-section~~ cross-section of a partially formed integrated circuit device having a structure formed during the practice of a method of the present invention.

Please amend the fourth full paragraph on page 7 as follows:

Figure 3 is a partial ~~cross-section~~ cross-section of a partially formed integrated circuit device for use with a method of the present invention.

Please amend the fifth full paragraph on page 7 as follows:

Figure 4 is a ~~cross-section~~ cross-section of the structure shown in Figure 3 after further processing, and having a structure formed by a method of the present invention.

Please amend the sixth full paragraph on page 7 as follows:

Figure 5 is a partial ~~cross-section~~ cross-section of a partially formed integrated circuit device showing features formed during the practice of a method of the present invention.

Please amend the seventh full paragraph on page 7 as follows:

Figure 6 is a partial ~~cross-section~~ cross-section of a partially formed integrated circuit device depicting facet etching of a bread-loafed dielectric on metallization lines.

Please amend the eighth full paragraph on page 7 as follows:

Figure 7 is a ~~cross-section~~ cross-section of the structure shown in Figure 5 after further processing, and having a structure formed by a method of the present invention.

Please amend the ninth full paragraph on page 7 as follows:

Figure 8 is a partial ~~cross-section~~ cross-section of a partially formed integrated circuit device showing features formed during the practice of a method of the present invention.

Please amend the first full paragraph on page 8 as follows:

Figure 9 is a ~~cross-section~~ cross-section of the structure shown in Figure 8 after further processing, having a structure formed by a method of the present invention.

Please amend the paragraph bridging pages 10 and 11 as follows:

One preferred method of forming a structure of the present invention includes providing a first dielectric layer 14 over the surface of a substrate ~~of an underling~~ or underlying layer 12, then forming a conductive layer 34 and an additional layer 36 thereover, as shown in Figure 3. Conductive layer 34 and additional layer 36 are then patterned by forming and patterning a mask layer over additional layer 36, and then etching additional layer 36, conductive layer 34, and a portion of first dielectric layer 14 at areas that are left exposed through the mask layer. This results in spaces between adjacent remaining portions of conductive layer 34.

Please amend the paragraph bridging pages 12 and 13 as follows:

Figure 6 illustrates an optional etch step that may be included immediately after deposition of additional layer 38 to remove lateral buildup of additional layer 38. The preferred etch is a facet etch, and is preferably performed in an argon or an ~~argon-plus-fluorine based~~ argon-plus-fluorine-based plasma. In a facet etch, additional layer 38 is etched slower at a top surface thereof than it is etched at a corner thereof which connects the top surface to a lateral surface thereof. The facet etch has the effect of removing substantially all of the lateral buildup portions of additional layer 38 and the removed portions redeposit in semi-triangular form at the base of the lines of conductive material 16 and first dielectric layer 14 interface. A continuous but thin lateral layer of additional layer 38 also deposits down the sides of lines of conductive material 16. Further processing as above then results in a structure like that which is shown in Figure 4, with the remaining portions of layer of additional material 36 corresponding to the remaining portions of additional layer 38. The redeposited fraction of additional material 38, however, remains thinly on the sides of lines of conductive material 16 and first dielectric layer 14.

Please amend the first full paragraph on page 14 as follows:

The preferred deposition process for selectively depositing a thin silicon dioxide layer 44 is an ~~ozone based~~ ozone-based TEOS process, which preferentially deposits on TiN over silicon dioxide. Preferably, silicon dioxide layer 44 will be deposited only on ~~titanium nitride~~ titanium nitride film 42 and not on the sidewall of aluminum lines 40 as shown in Figure 8.

Please amend the third full paragraph on page 14 as follows:

As an alternative process step, an etch such as a facet etch in an argon or an ~~argon-plus-fluorine based~~ argon-plus-fluorine-based plasma may be performed on silicon dioxide layer 44 after the deposition thereof.